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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,420	10/11/2001	Jong-Keun Ahn	8836-143 (IB11007-US)	9085

7590 09/14/2004

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EXAMINER	
SHUTE, DOUGLAS M	
ART UNIT	**PAPER NUMBER**
2121	4

DATE MAILED: 09/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/975,420	Applicant(s) AHN, JONG-KEUN	
	Examiner Douglas M. Shute	Art Unit 2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/11/01* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 are presented for examination.

Drawings

2. In Figure 1, the HV line output from element 210 appears to be labeled as "Write Buffer". Clarification is required.

3. In Figures 1, 4, and 5, the meaning of the dotted portion of element 180 (write buffer) is unclear in the specification. Correction is required.

4. In addition, in Figures 1, 4, and 5, the interconnection between element 220 (data register) and element 180 (write buffer) is shown as a multiple line interconnection (i.e., by slash). The specification, for example, however recites "serially transferring a group of data bits to the nonvolatile memory …" (page 4, line 14). This serial transfer of data would imply a single line interconnection as opposed to the multiple lines illustrated. Clarification is required.

Specification

5. The disclosure is objected to because of the following informalities: On page 9, line 21 and page 11, line 11, reference is made to a time value of 30 seconds which appears to be inconsistent with the remainder of the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in

the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, the mechanism or steps by which data is transferred from the controller to the nonvolatile memory is unclear. In addition, there appears to be a discrepancy between claims 1 and 8, for example, and Figures 1, 4, and 5 as to whether this is a serial or parallel transfer. Claim 1 (and specification, page 4) recites "transferring the first group of serial bits to the nonvolatile memory …". Claim 8 (and specification, page 4) recites "serially transferring a group of data bits to the nonvolatile memory …". In contrast to claims 1 and 8, Figures 1, 4 and 5 show the schematic representation of a multi-line connection (i.e. by slash) between element 220 (data register) and element 180 (write buffer) indicative of a parallel connection. Clarification is required.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 2, 8, 10, 11, 12, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, claims 2, 8, 12, and 15 recite "determining the capacity of the nonvolatile memory". In contrast, the specification appears to utilize the determination of the write data bus width or the write buffer size (e.g., page 8, lines 8-9) vs. the capacity of the entire nonvolatile memory. Claim 8 is also rejected as it recites "while transferring a next group of data bits to the nonvolatile memory". The specification indicates that the next group of data bits is transferred to the controller while programming the nonvolatile memory. Claim 10 recites an "embodied voltage generator" which is unclear. Claim 11 recites "performing of the stored data bits" which is unclear. Clarification of all is required.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1, 3-6 and 8-17, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Futatsuya et al. (6,483,748) (hereinafter Futatsuya) in view of Devore et al. (5,432,741) (hereinafter Devore) and in further view of Oguro et al. (5,790,572) (hereinafter Oguro).

12. As per claims 1 and 4, as best understood, Futatsuya shows the invention substantially as claimed having a method for programming a nonvolatile memory (e.g., figure 1, elements MA

and associated text) by a control system having a controller for controlling transfer of data to be programmed (e.g., figure 1, elements 1, 2, and 7 and associated text), the method comprising the steps of:

sequentially transferring and storing address bits from the exterior to the controller (e.g., figure 1, element 1 and associated text);

sequentially transferring and storing a first group of data bits from the exterior to the controller (e.g., figure 1, element 2 and associated text);

transferring the first group of serial data bits to the nonvolatile memory (e.g., figure 1, element 4 and associated text). Futatsuya does not specifically show that the transfer and storing of data and address information from the exterior to the controller is a serial transfer. Devore shows such a serial transfer of data from the exterior to a controller (e.g., figure 1, elements 10 and 12 and interconnections thereto). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the serial transfer mode of Devore could be utilized in the system of Futatsuya to provide an efficient way of transferring data utilizing minimum hardware for interconnetions. Futatsuya also does not specifically show determining whether all the serial data bits of the first group

are transferred to the controller. However, Oguro shows data transfer upon detection of a stop bit indicative of receipt of all desired data (e.g., col. 1, lines 48-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the conditional data transfer dependent on a stop bit as shown in Oguro could be utilized in the system of Futatsuya in order to provide an enhanced data transfer having increased assurance that all desired data had been received prior to transfer. Futatsuya also does not specifically show sequentially transferring and storing a second group of serial data bits to the controller, while programming the first group of serial data bits in the nonvolatile memory at the address indicated by the address bits. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the structure of Futatsuya could be optimally utilized in such a fashion to simultaneously program a first set of data (e.g., from figure 1, element 4) while storing a second set of data in the controller (e.g., in figure 1, element 2) thereby providing overall reduction in transfer time.

13. As per claim 3, as best understood, it is rejected for reasons as given above for claim 1. Further Futatsuya shows generating a voltage enable signal necessary for the programming

(e.g., col. 8, lines 37-40 and figure 1, dashed line from element 7 to element 25). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the generating of the voltage enable signal could take place before the step of programming the first group of serial data bits in the nonvolatile as this would be a necessary requirement for timely and accurate programming of the nonvolatile memory.

14. As per claim 5, as best understood, it is rejected for reasons given above for claim 1 and further as it would have been obvious to one of ordinary skill in the art at the time the invention was made the address could be increased whenever all the serial data bits of the respective group, except the serial data bits of the first group, are transferred to the controller as the incrementing of addresses to determine the location of succeeding groups of data in multiple data group transfer is a well-known mechanism.

15. As per claim 6, as best understood, it is rejected for reasons as given above for claim 1 and further as it would have been obvious to one of ordinary skill in the art at the time the invention was made that each group of the serial data bit could

comprise 1 byte or more as bytes are a typical and well-known grouping of data used in data transfer such as those used in memory manipulations.

16. As per claim 8, as best understood, it is rejected as being essentially a control system analogous to the method rejected in claim 2. In addition, Futatsuya shows a memory chip having a nonvolatile memory for storing data bits and programming the stored data bits (e.g., figure 1, elements 4, 25 and MA). Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the system could
serially transfer a group of data bits to the nonvolatile memory based on the capacity of the nonvolatile memory as this would permit efficient and flexible transfer of data dependent upon the variable enable period as described in the rejection of claim 2.

17. As per claim 9, as best understood, it is rejected for reasons as given above for claim 8 and further as Futatsuya shows (e.g., figure 1, element 4) a write buffer for receiving and storing the group of data bits from the controller, and

transferring the stored group of data bits to the nonvolatile memory.

18. As per claim 10, as best understood, it is rejected for reasons as given above for claim 9. Further, Futatsuya shows a voltage generator for generating a voltage necessary for the programming in the nonvolatile memory (e.g. figure 1, element 7 which produces dotted line signal between element 7 and 25). It would have been obvious to one of ordinary skill in the art at the time the invention was made that this generator could be located anywhere in the system as a particular circumstance warranted (such as within the memory chip).

19. As per claim 11, as best understood, it is rejected for reasons as given above for Claim 8. Further, Futatsuya shows a data register for storing the group of data bits serially provided from exterior and transferring the group of data bits to the write buffer, the group of data bits being programmed in the nonvolatile memory (e.g., figure 1, element 2);
an address register for storing address bits serially provided from exterior, and transferring the stored address bits to the nonvolatile memory (e.g., figure 1, element 1); and

a control logic for making the group of data bits and address bits in the data and address registers transferred to the write buffer and the nonvolatile memory respectively and enabling a program enable signal for the performing of the stored data bits in the nonvolatile memory (e.g., figure 1, elements 7 and signals CTL and CMD connected thereto). Futatsuya does not specifically show the address bits are varied when the next group of data bits is transferred to the data register but it would have been obvious to one of ordinary skill in the art at the time the invention was made that the address bits could be varied when the next group of data bits is transferred to the data register as the incrementing of addresses to determine the location of succeeding groups of data in multiple data group transfer is a well-known mechanism.

20. As per claim 12, as best understood, it is rejected for reasons as given above for claim 11 and further as it would have been obvious to one of ordinary skill in the art at the time the invention was made that the controller could further comprise a byte select circuit for outputting a byte select signal indicating the capacity of the nonvolatile memory, wherein the control logic controls an enable period of the program enable signal based upon the byte select signal as such a byte select

circuit would be a convenient means of holding a value indicative of the nonvolatile memory capacity.

21. As per claim 13, as best understood, it is rejected for reasons as given above for claim 12 and further as it would have been obvious to one of ordinary skill in the art at the time the invention was made that the transferring time of the group of serial data bits is the same or is longer than the enable period of the program enable signal as an equal transferring time and program enable signal period would be the anticipated mode of typical operation.

22. As per claim 14, as best understood, it is rejected for reasons as given above for claim 12 and further as it would have been obvious to one of ordinary skill in the art at the time the invention was made that the byte select circuit could set the byte select signal before the transferring of the address bits and the group of data bits are
started as the timing of this signal setting could occur in any number of places in the overall programming cycle as a particular circumstance warranted.

23. As per claim 15, as best understood, it is rejected for reasons as given above for claim 12 and further as it would have been obvious to one of ordinary skill in the art at the time the invention was made that the controller could further comprise a command register for receiving information for the capacity of the nonvolatile memory as this would provide an externally accessible location for receiving desired memory capacity as a particular circumstance warranted.

24. As per claim 16, as best understood, it is rejected for reasons as given above for claim 15 and further as it would have been obvious to one of ordinary skill in the art at the time the invention was made that the byte select circuit could set the byte select signal according to the information of the command register as the byte select circuit could act as a less transient storage facility of memory capacity information with respect to the command register whose contents could be readily varied as desired prior to actual incorporation of its contents in the overall nonvolatile memory programming process as a particular circumstance warranted.

25. As per claim 17, as best understood, it is rejected for reasons as given above for claim 12 and further as it would have

been obvious to one of ordinary skill in the art at the time the invention was made that the byte select circuit could set the byte select signal by using one of a central processing unit of the control system and a ground voltage pin as these represent any number of potential input signal sources which would provide a desired byte select circuit as a particular circumstance warranted.

26. Claim 2, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Futatsuya et al. (6,483,748) (hereinafter Futatsuya) in view of Devore et al. (5,432,741) (hereinafter Devore) and in further view of Oguro et al. (5,790,572) (hereinafter Oguro) and in further view of Shaberman et al. (5,761,732)(hereinafter Shaberman).

27. As per claim 2, as best understood, it is rejected for reasons as given above for claim 1. Further, the combination of Futatsuya, Devore and Ogurao does not specifically show before the step of transferring the serial address bits to the controller, the steps of:
determining the capacity of the nonvolatile memory; and
setting an enable period of the programming in the nonvolatile memory according to the result of the step of determining the

capacity of the nonvolatile memory. However, Shaberman shows the use of a data bus indicator signal in a memory interface (e.g., col. 6, lines 14-16). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the data bus width indicator signal described in Shaberman could then be utilized to produce a corresponding programming enable period which would provide a more flexible mechanism by which to program nonvolatile memories of different bus widths. It would have been further obvious to one of ordinary skill in the art at the time the invention was made that this memory capacity determining and enable period setting could take place prior to transferring the serial address bits to the controller as a particular circumstance warranted.

28. Claim 7, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Futatsuya et al. (6,483,748) (hereinafter Futatsuya) in view of Devore et al. (5,432,741) (hereinafter Devore) and in further view of Oguro et al. (5,790,572) (hereinafter Oguro) and in further view of Tsai (6,009,496) (hereinafter Tsai).

29. As per claim 7, as best understood, it is rejected for reasons as given above for claim 1. Further, the combination of Futatsuya, Devore and Oguro does not specifically show the nonvolatile memory is embodied in the control system. Tsai shows a microcontroller with embedded flash memory. It would have been obvious to one of ordinary skill in the art at the time the invention was made that the nonvolatile memory as claimed could be incorporated in the control system as a particular circumstance warranted.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas M. Shute whose telephone number is (703) 305-5615 (571-272-3690 on or about 10/26/04). The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on (703) 308-3179 (571-272-3687 on or about 10/14/04). The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 13, 2004

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